



**FEATURES:**

- PFD input frequency range: 5 MHz to 100 MHz
- Output frequency range: 20 MHz to 600 MHz
- Operating voltage range: 1.6 V to 2.0 V
- Operating junction temperature: -40° C to 125° C
- Area: 400 μm X 270 μm
- Pre-divider ratios: 1, 2, 4, 8
- Loop-divider Dy range: 2 to 32
- Built-in loop filter
- Power-down mode
- Built-in lock detection
- Built-in ring oscillator
- By-pass mode

**APPLICATIONS:**

- Clock multiplication, clock generation

**TECHNOLOGY:**

- CHRT 0.18 μm generic IB CMOS

**STATUS:**

- MPW in progress

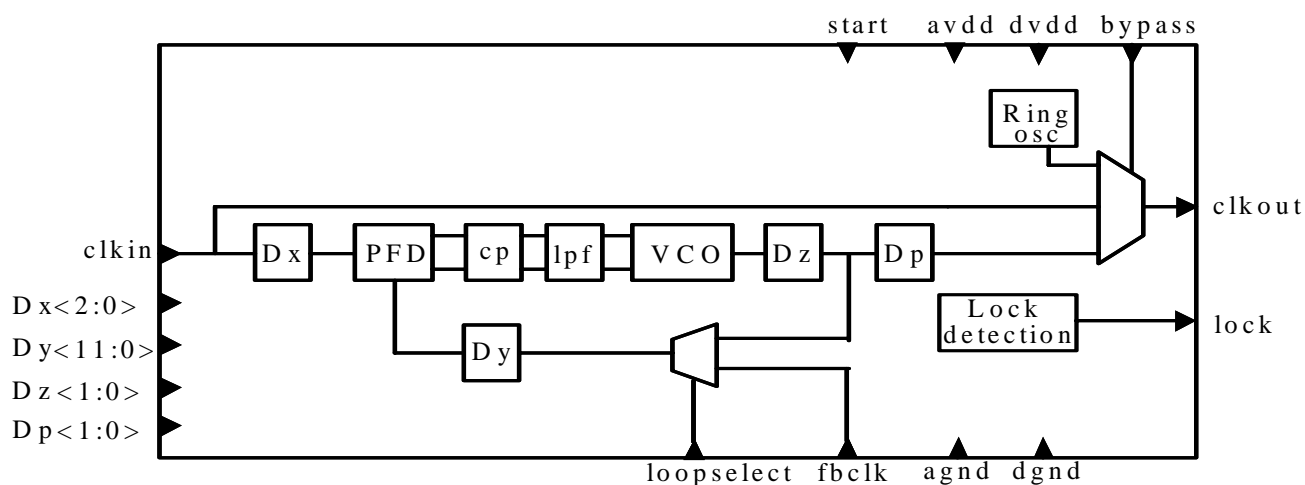
**JITTERS:**

- Peak-to-peak period jitter:
- RMS period jitter:

**Brief description**

The Haokai\_PLL\_180CHRT\_02, a 0.18 μm phase locked loop (PLL), provides a clock generation and multiplication circuit that generates a stable, high-speed clock from a clock signal with medium frequency (5 MHz to 100 MHz). A differential VCO architecture together with a unique charge pump design ensures that the PLL jitter is small. Differential VCO output can be converted into a single-ended output clock with the same frequency while maintaining its 50% duty cycle. This will ensure low power consumption for the PLL. Loop divider Dy can be selected with any integer numbers between 2 and 32.

**FUNCTIONAL DIAGRAM**



*Dx can be 1, 2, 4, 8; Dz can be 1, 2, 4; Dp can be 1, 2, 4, 16; Dy can be set from 2 to 32*

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