



FEATURES:

- PFD input frequency range: 5 MHz to 400 MHz
- Output frequency range: 10 MHz to 800 MHz
- Operating voltage range: 1.08 V to 1.32 V
- Operating junction temperature: -40° C to 125° C
- Area: 260 μm x 525 μm
- Pre-divider ratios: 1, 2, 3...32
- Post-divider ratios: 1, 2, 3...32
- Loop-divider Dy range: 1, 2, 3....512
- Deskew mode and frequency synthesise mode
- Total 3 clock outputs
- 2 clock outputs are 360 degree phase adjustable (phase adjustment step is 1/10th of a VCO clock)
- Built-in lock detection and by-pass mode

APPLICATIONS:

- FPGA PLL

TECHNOLOGY:

- SMIC130 nm generic 1.2V CMOS

STATUS:

- MPW in progress

JITTERS:

- To be measured

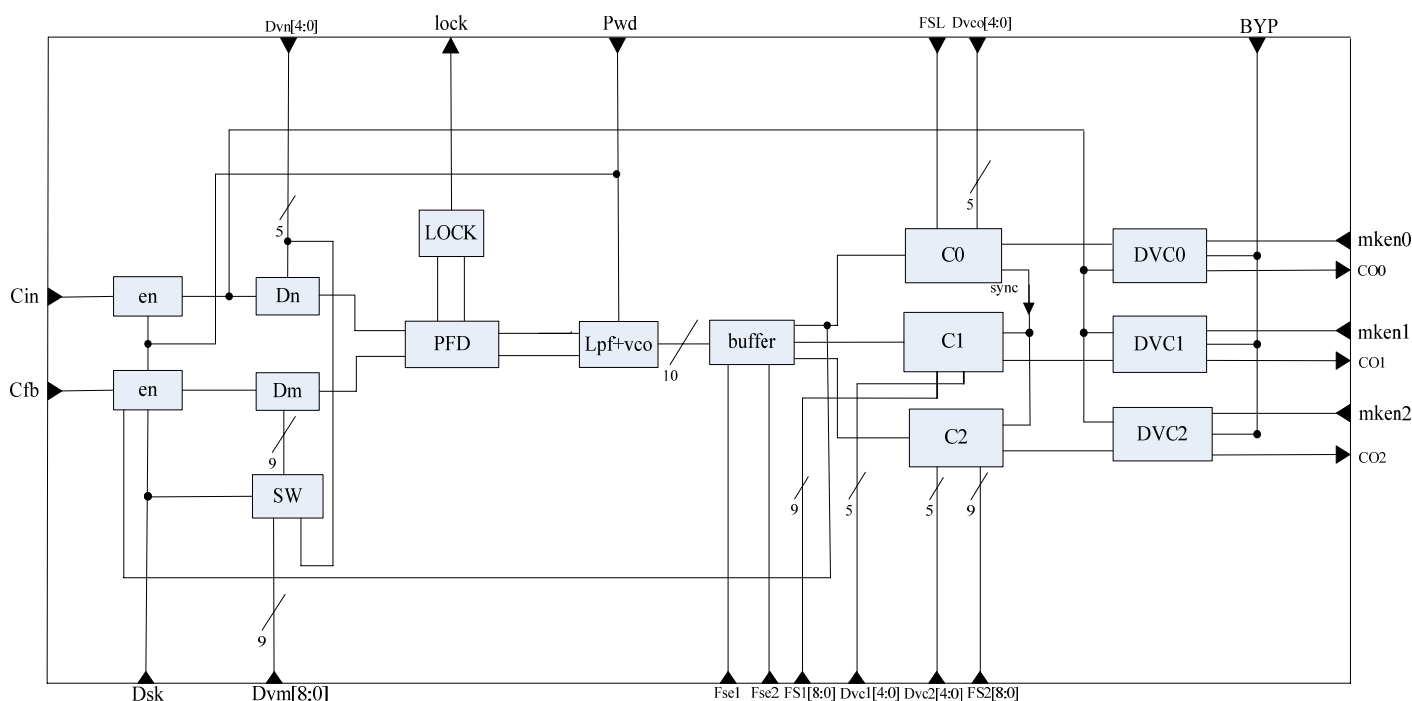
Power:

- 15 mA at worst-case setting (simulated)

Brief description

Haikai_PLL_130_FPGA_SMIC_01, a 130 nm low-jitter phase locked loop (PLL) IP, specifically designed for FPGA applications, provides clock generation, clock multiplication, and deskewing functions. This PLL features super wide input and output frequency ranges. A differential VCO architecture together with a unique charge pump and loop filter design ensures that the PLL jitter is small. Differential VCO output can be converted into a single-ended output clock with the same frequency while maintaining its 50% duty cycle. Loop divider Dm can be selected with any integer numbers between 1 and 512. PLL stability can also stand large temperature, voltage, and process variations. Using special power noise rejection technology, analog power noise is mostly filtered out. Analog power/ground pins can be connected directly to digital power/ground pins, with some jitter performance degradation. The PLL has 3 clock outputs. 2 of the 3 output clocks are 360 degree phase adjustable with phase adjustment step as fine as 1/10th of a VCO clock.

FUNCTIONAL DIAGRAM



Dn can be 1,2,3...,32; DVC# can be 1, 2, 3...,32; Dm can be 1, 2, 3...,512.

Pin function table

Pin Name	Description	I/O	Pin
Cin	Reference clock 10-350MHz	in	1
Cfb	Feedback clock: used in deskew mode	in	1
CO0	Main output clock	out	1
CO1	First shifted phase out clock Can run at different freq in synthesizer mode	out	1
CO2	Second shifted phase out clock Can run at different freq in synthesizer mode	out	1
Lock	Lock status output	out	1
Pwd	Power down. Disable all outputs and no power. PLL quiet	in	1
Dsk	Deskew enable: Cfb selected as feedback. Dsk will force Dvm[1:512] = Dvn[1:32] . it will also force Dvc1[1:32] and Dvc2[1:32] to be the same as Dvc0[1:32] to make deskew possible for all three output clocks	in	1
Byp	Bypass input to output of Co0/Co1/Co2 when they are enabled. Bypass will also shut off all of PLL in deskew mode. Under frequency synthesizer mode, PLL feedback can still be present	in	1
Mken0	Output enable for CO0. it will be forced to be 1 to enable feedback loop in deskew mode	in	1
Mken1	Output enable for CO1	in	1
Mken2	Output enable for CO2	in	1
Fse1*	Phase shift enable for CO1	in	1
Fse2*	Phase shift enable for CO2	in	1
FSL*	Phase shift linked between 3 outputs CO0, CO1, and CO2: phase relationship will be established between Co0 and Co1, or between Co0 and Co2.	in	1
Dvn[4:0]	N: Input reference divider control	in	5
Dvm[8:0]	M: feedback clock divider control, will be forced to be equal to N under deskew mode	in	9
Dvc0[4:0]	C0 divider control	in	5
Dvc1[4:0]	C1 divider control; under deskew mode, C1 and C2 are forced to equal to C0	in	5
Dvc2[4:0]	C2 divider control; under deskew mode, C1 and C2 are forced to equal to C0	in	5
Fs1[8:0]	CO1 phase shift control: [8:5] are used to select VCO output into C1 divider, only 10 out of 16 states used. [4:0] are used to select different phases from C1 dividers. For divide by 1, 2, 4, 8, 16, 32, none, or [0],[1:0], [2:0],[3:0], [4:0] are used, respectively, to select different phases from the programmable divider.	in	9
Fs2[8:0]	CO2 phase shift control: [8:5] are used to select VCO output into C2 divider, only 10 out of 16 states used. [4:0] are used to select different phases from Dvc1 dividers. For divide by 1, 2, 4, 8, 16, 32. None or [0],[1:0], [2:0],[3:0], [4:0] are used, respectively, to select different phases from the programmable divider.	in	9

Frequency equations:

$$Output_frequency = \frac{input_frequency \times Dm}{Dn \times Dvc0}$$

$$VCO_frequency = Output_frequency \times Dvc0$$

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