



FEATURES:

- PFD input frequency range: 0.5 MHz to 250 MHz
- Output frequency range: 20 MHz to 1 GHz
- Operating voltage range: 1.08 V to 1.32 V
- Operating junction temperature: -40° C to 125° C
- Area: 405 μm X 314 μm
- Pre-divider ratios: 1, 2, 4, 8, 16, 32, 64, 128
- Loop-divider Dy range: 2 to 512
- Built-in loop filter
- Power-down mode
- Built-in lock detection
- Built-in ring oscillator
- By-pass mode

APPLICATIONS:

- Clock multiplication, clock generation

TECHNOLOGY:

- CHRT 0.13 μm generic CMOS

STATUS:

- Silicon proven on MPW

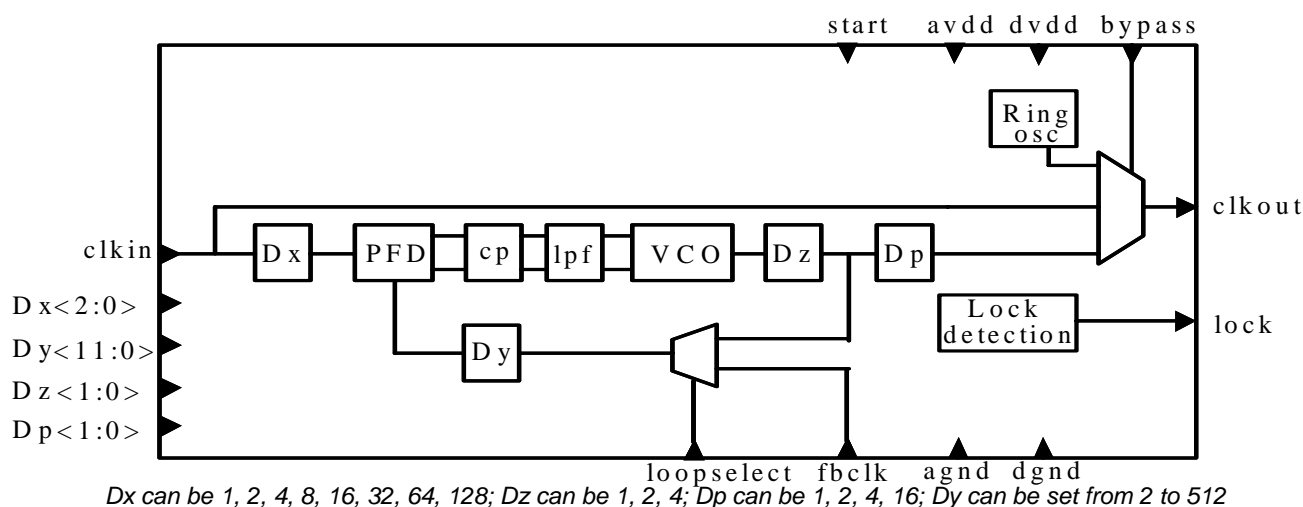
JITTERS:

- Peak-to-peak period jitter: 18 ps - 288 ps
- Peak-to-peak period jitter: 0.7% - 4.6%
- RMS period jitter: 2.2 ps - 70 ps
- RMS period jitter: 0.1% - 0.8%

Brief description

The Haokai_PLL_130CHRT_02, a 0.13 μm phase locked loop (PLL), provides a clock generation and multiplication circuit that generates a stable, high-speed clock from a clock signal with very high input frequency (0.5 MHz to 250 MHz). A differential VCO architecture together with a unique charge pump design ensures that the PLL jitter is small. Differential VCO output can be converted into a single-ended output clock with the same frequency while maintaining its 50% duty cycle. This will ensure low power consumption for the PLL. Loop divider Dy can be selected with any integer numbers between 2 and 512.

FUNCTIONAL DIAGRAM



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