



FEATURES:

- PFD input frequency range: 0.5 MHz to 5 MHz
- Output frequency range: 20 MHz to 1.6 GHz
- Operating voltage range: 0.9 V to 1.1 V
- Operating junction temperature: -40° C to125° C
- Area: 289 μm X 255 μm
- Pre-divider ratios: 1, 2, 4, 8, 16, 32, 64, 128
- Post-divider ratios: 1, 2, 4, 16
- Loop-divider Dy range: 200 to 3200
- Built-in loop filter
- Power-down mode
- Built-in lock detection
- Built-in ring oscillator
- By-pass mode

APPLICATIONS:

- Clock multiplication, clock generation; Various SOC and ASIC design, CPU etc

TECHNOLOGY:

- SMIC 90 nm generic 1.0V/3.3 V CMOS

STATUS:

- Silicon proven on MPW

JITTERS:

- Peak-to-peak period jitter: 15 - 38 ps
- Peak-to-peak period jitter: 0.74% - 4.46%
- RMS period jitter: 2 - 7 ps
- RMS period jitter: 0.12% - 0.48%

Brief description

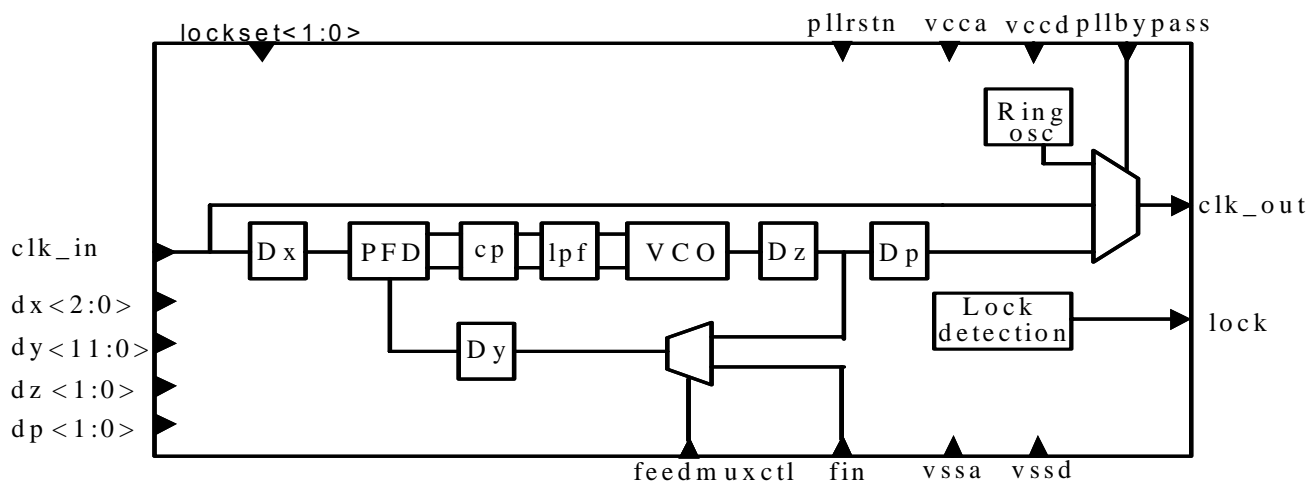
The Haokai_PLL_090SMIC_01, a 90 nm phase locked loop (PLL), provides a clock generation and multiplication circuit that generates a stable, high-speed clock from a clock signal with very low input frequency range (0.5 MHz to 5 MHz). A differential VCO architecture together with a unique charge pump design ensures that the PLL jitter is small. Differential VCO output can be converted into a single-ended output clock with the same frequency while maintaining its 50% duty cycle. This will ensure low power consumption for the PLL. Loop divider Dy can be selected with any integer numbers between 200 and 3200.

No special connection required for PLL IPs with SMIC-IO. Analog power/ground pins can either be directly from outside pins or connected to regulated power/ground on die.

Due to special power noise rejection technology, analog power noise is mostly filtered out, analog power/ground pins can be connected directly to digital power pins too, with some jitter performance degradation.

Digital power pins can be directly connected to digital power net on chip. Share the same power with other digital circuit.

FUNCTIONAL DIAGRAM



dx can be 1, 2, 4, 8, 16, 32, 64, 128; dz can be 1, 2, 4; dp can be 1, 2, 4, 16; dy can be set from 200 to 3200

The detailed explanation of each signal usage

Pin name	DIR	Description
vcca	P	Dedicated analog power supply 1v
vccd	P	Dedicated digital power supply 1v
vssa	G	Dedicated analog ground
vssd	G	Dedicated digital ground
clk_in	I	Reference clock input from Crystal Oscillator or other clock sources
clk_out	O	PLL output clock
dx<2:0>	I	Input 3-bit divider control pins, dx<0> is LSB
pllrstn	I	Pllrstn=1 should be used in normal PLL operation, Pllrstn=0 power down control
dp<1:0>	I	Output 2-bit divider control pins, dp<0> is LSB
dy<11:0>	I	Feedback 12-bit integral divider control pins, dy<0> is LSB
pllbyypass	I	Bypass the PLL; Active high
feedmuxctl	I	External feedback loop selection; Active high
lockset<1:0>	I	PLL lock detector control pins. 11 for normal mode
dz<1:0>	I	VCO to output 2-bit integral divider control pins
lock	o	Locked signal (high for locked)
fin	I	Input frequency for the custom to break the loop

The equation of the output frequency :

$$clk_out = \frac{clk_in \times dy}{dx \times dp}$$

$$VCO = clk_out \times dz$$

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