

# Haokai Microelectronics (Shanghai) Corporation

[www.haokai-micro.com](http://www.haokai-micro.com)

**Phase-locked loop (PLL) IP**

**Phase-locked loop (PLL) design service**

**Phase-locked loop (PLL) chip products**



Haokai Microelectronics (Shanghai) Corporation

# Outline

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  - Phase-locked loop (PLL) IP
  - Phase-locked loop (PLL) design service
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# Company introduction

## ❖ Company Info

- Founded at Shanghai in May 2005
- Number of employees: 12

## ❖ Core business

- Phase-locked loop (PLL) silicon IP (SIP)
- Phase-locked loop (PLL) design service
- Phase-locked loop (PLL) chip products

## ❖ Mission

- To be the leading provider for phase-locked loop (PLL) IP, design service, and chip products to the worldwide semiconductor design houses and manufacturers



# Management team

- ❖ CEO: Dr. Cangsang Zhao
  - B.S. in Physics from Peking Univ., Ph.D. in EE in USA
  - Worked in Intel USA for 9 years, as a senior designer, a design manager, and a senior design manager etc.
  - Involved in the design of Intel Pentium III、 IV、 和IV dual core
  - Authored and co-authored 15 papers in international conferences and Journals
  - Held 7 U.S. patents
  
- ❖ CTO: Dr. Feng Wang
  - B.S. in Physics from Peking Univ., Ph.D. in Physics in USA
  - Worked in Intel USA for 9 years, as a senior designer, accumulated enormous analog and mixed signal design experience.
  - Involved in the design of Intel Pentium III、 IV、 和IV dual core
  - Held 3 U.S. patents



# Core business: PLL SIP

- ❖ High-speed, low-jitter phase-locked loop (PLL) SIP
  - 0.18 um to 0.09 um CMOS process
  - Output clock up to 3 GHz
  - Typical low jitter noise down to 20ps/3ps (peak-to-peak/RMS)
  
- ❖ Existing PLL IPs in SMIC
  - Universal PLL on SMIC 0.13 um CMOS , silicon-proven
    - Input range: 2 MHz to 800 MHz
    - Output range: 20 MHz to 1.6 GHz
    - Divider range: 2 to 4096
  - 2.8GHz PLL on SMIC 0.13 um CMOS , silicon-proven
  - 3 GHz PLL on 90 nm CMOS , silicon-proven
  - On SMIC 0.13 um generic CMOS, PLL IP for FPGA ICs, under development
  
- ❖ Existing PLL IPs in Chartered Semiconductor Manufacturing
  - 1GHz PLL on Chartered 0.13 um CMOS, silicon proven
  - Universal PLL on Chartered 0.13 um CMOS, silicon proven
    - Input range: 2 MHz to 200 MHz
    - Output range: 20 MHz to 1.1 GHz
    - Divider range: 2 to 512
  - 1 Ghz PLL on Chartered 0.18 um CMOS, under development



# Core business: Design service

- ❖ PLL IP custom design
- ❖ PLL design service for clock chips
- ❖ LC—VCO design and development



# Core business: Chip products

- ❖ Haokai is developing Programmable clock chips for applications in the area of consumer, communication, and computer electronics



# Growth path

- ❖ **2005/05**: Haokai registered in Zhangjiang, Shanghai, China.
- ❖ **2005/06**: Haokai obtained its first project – to design a high speed PLL and a set of HSTL IOs
- ❖ **2005/11**: Haokai's project “The design and development of high-end analog, mixed-signal, and IO IPs” obtained a technology-innovation funding from Pudong government
- ❖ **2005/12**: Haokai signed contract “Cooperating on developing and testing PLL IPs” with SMIC
- ❖ **2006/5**: Haokai successfully developed a 3.5 GHz PLL and 300 MHz HSTL-IO on SMIC 0.13 um CMOS process, and demonstrated the highest speed PLL developed in China on its first try.
- ❖ **2006/09**: Haokai's project “90 nm CMOS high speed PLL” obtained Shanghai government “Deng Shan Xing Dong Ji Hua” funding.
- ❖ **2006/11**: Haokai’s project “Digitized high speed PLLs” obtained Shanghai and national innovation funding support



# Growth path cont.

- ❖ **2007/09**: Haikai's project "Low power, low jitter, wide-range PLL IPs" obtained Shanghai government's "Pu Jiang Ren Cai" funding support
- ❖ **2007/10**: Haikai introduced low jitter silicon-proven PLL IPs on SMIC's 0.13 um Mixed signal CMOS process
- ❖ **2007/11**: Haikai introduced low jitter silicon-proven PLL IPs on SMIC's 90 nm generic CMOS process
- ❖ **2007/11**: Haikai signed contract with Chartered Semiconductor to cooperate on developing PLL IPs
- ❖ **2007/12**: Haikai successfully passed government's checking on project "90 nm CMOS high speed PLL"
- ❖ **2008/03**: Haikai introduced low jitter silicon-proven PLL IPs on SMIC's 0.13 um generic CMOS process
- ❖ **2008/04**: Haikai introduced low-jitter silicon-proven PLL IPs on Chartered Semiconductor's 0.13 um generic CMOS process
- ❖ **2008/08**: Haikai is developing a PLL IP for FPGA ICs



# Partners

- ❖ Semiconductor Manufacturing International Corporation (SMIC)
  - Haokai Microelectronics signed contract “Cooperating on developing and testing PLL IPs” with SMIC
- ❖ Chartered Semiconductor Manufacturing Corporation
  - Working with Chartered to develop PLL IP on 0.18 um and 0.13 um CMOS processes
- ❖ Shanghai SIP Exchange (SSIPEX)
  - SSIPEX is Haokai’s IP distributor
- ❖ Ministry of Information Industry Software and Integrated Circuit Promotion Center (CSIP)
  - CSIP is Haokai’s IP distributor



# Contact us

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# Thank You !

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